UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,417	02/23/2004	Minchang Liang	A1385	1815

45851 7590 05/19/2005

G. VICTOR TREYZ
FLOOD BUILDING
870 MARKET STREET, SUITE 984
SAN FRANCISCO, CA 94102

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,417	LIANG ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *6-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 18* is/are rejected.

7)☒ Claim(s) *1,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-23-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed May 2, 2005.

Election/Restrictions

Applicant's election without traverse of claims 1-5 and 18-20 in the reply filed on May 2, 2005 is acknowledged.

Claim Objections

Claim 1 is objected to because of the following informalities: "**gate oxide layer**" should have been **gate dielectric layer** in line13. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Okuno et al. (US 6,803,634 B2).

In regard to claim 1, Okuno et al. teach a complementary-metal-oxide-semiconductor integrated circuit 34 comprising: a metal-oxide-semiconductor (MOS) field- effect transistor having a source 43, a drain 43, and a gate 45 having a gate dielectric layer 44; and a bipolar transistor 35 having an emitter 49, a collector 51, and a base 50, wherein the base 50 has: a base region with a width that separates the emitter 49 and collector 51 and a length, and a base conductor 47 that is electrically connected to the base region along its length without being blocked by intervening portions of the gate oxide layer 44 (Figure 1, columns 4-5, lines 10-67 and 1-33, respectively).

In regard to claim 4, Okuno et al. teach a semiconductor substrate 32 from which the MOS transistor 34 and bipolar transistor 35 are formed, wherein the semiconductor substrate 32 comprises a silicon- on-insulator (SOI) substrate 32, 33, 36 & 37 (Figure 1, column 4, lines 10-67).

In regard to claim 18, Okuno et al. teach a complementary-metal-oxide-semiconductor-integrated-circuit bipolar transistor 31 on a complementary-metal-oxide-semiconductor (CMOS) integrated circuit having a semiconductor substrate 32, comprising: an emitter having an emitter region 49 in the semiconductor substrate 32 of the CMOS integrated circuit; a collector 51 having a collector region in the semiconductor substrate 32 of the CMOS integrated circuit; and a base 50 having: a base region in the semiconductor substrate 32 of the CMOS integrated circuit that lies between the emitter region 49 and the collector region 51, wherein the base region 50 has a length and a width and wherein the emitter region 49 and the collector region 51

are separated by the width of the base region 50, and a base conductor 47 that lies above the base region 50 and that is electrically connected to the base region 50 along its length (Figure 19B), wherein the base conductor 47 serves as a path for base current in bipolar transistor 35 (Figure 1, columns 4-5, lines 10-67 and 1-33, respectively).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. (US 6,803,634 B2) as applied to claims 1, 4 and 18 above, and further in view of Furukawa et al. (US 2003/0104658 A1).

Okuno et al. teach all mentioned in the rejection above.

However, Okuno et al. fail to teach the base conductor comprises doped semiconductor patterned from a crystalline semiconductor epitaxial layer grown on the base region.

Furukawa et al. teach a base conductor 84 comprising doped semiconductor (Figure 16, page 5, paragraph [0060]).

In regard to the base conductor being patterned from a crystalline semiconductor epitaxial layer grown on the base region, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the

product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the complementary-metal-oxide-semiconductor integrated circuit structure as taught by Okuno et al. with the complementary-metal-oxide-semiconductor integrated circuit having a base conductor comprising doped semiconductor as taught by Furukawa et al. to provide a method and structure for integrating CMOS and bipolar transistors (page 1, paragraph [0005]).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. (US 6,803,634 B2) as applied to claims 1, 4 and 18 above, and further in view of Iranmanesh (EP 0 450 376 A1).

Okuno et al. teach all mentioned in the rejection above.

Okuno et al. further teach a gate conductor 45 formed on tope of the gate dielectric layer 44 from polysilicon (Figure 1, column 4, lines 32-39).

However, Okuno et al. fail to teach the gate comprising a gate conductor formed on top o the gate dielectric layer from polysilicon and silicide or from metal; and the base conductor comprising silicide.

Iranmanesh teaches the gate conductor and the base conductor comprising silicide (abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the complementary-metal-oxide-semiconductor integrated circuit structure as taught by Okuno et al. with the complementary-metal-oxide-semiconductor integrated circuit having gate and base conductors comprising silicide as taught by Iranmanesh to achieve improved performance (abstract).

Allowable Subject Matter

Claims 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to complementary-metal-oxide-semiconductor integrated circuits:

Chang et al. (5,504,364)

Kihara et al. (5,286,986)

Kouno et al. (US 6,365,932 B1)

Maeda et al. (5,399,894)

Matthews (5,336,926).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
May 13, 2005